Amendments to the Claims

This listing of claims will replace all prior versions, and listing, of claims in the application:

1.   (Currently Amended) A method for detecting whether an IDE drive is connected to an intelligent drive electronics channel within a computer, comprising:

writing data to a drive head register destination for the IDE drive;

in response to writing the data to the drive head register destination, reading the drive head register destination;

detecting whether the data read from the drive head register destination matches the data written to the drive head register destination;

in response to the data read from the drive head register destination not matching the data written to the drive head register destination, returning that the IDE drive is not connected to an intelligent drive electronics channel;

in response to the data read from the drive head register destination matching the data written to the drive head register destination, reading the status register destination;

reading a status register destination for the IDE drive; ~~and~~

detecting whether data read from the status register destination has a first predefined value;

upon the data read from the status register destination not having the first predefined value, returning that the IDE drive is connected to the intelligent drive electronics channel~~determining whether the IDE drive is connected based on a value read from the status register destination~~;

upon the data read from the status register destination having the first predefined value, reading a cylinder low register destination and a cylinder high register destination of the drive;

detecting whether data read from the cylinder low register destination and the cylinder high register destination matches a predefined signature; and

in response to the data read from cylinder low register destination and the cylinder high register destination matching the predefined signature, returning that the IDE drive is connected to the intelligent drive electronics channel.

2.   (Cancelled).

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3.   (Cancelled)

4.   (Previously Presented)   The method of claim 1, further comprising:

prior to writing data to a drive head register destination for the IDE drive, establishing a drive selection value for each IDE drive; and

selecting the IDE drive for detection by writing a drive selection value to the drive head register destination.

5.   (Cancelled).

6.   (Currently Amended) The method of claim 5̶1, wherein the IDE drive connected to the intelligent drive electronics channel implements a packet command feature set.

7.   (Currently Amended) The method of claim 5̶1, further comprising in response to the data read from cylinder low register destination and the cylinder high register destination not matching the predefined signature, returning that the IDE drive is not connected to an intelligent drive electronics channel.

8.   (Original)   The method of claim 7, wherein the predefined signature comprises a second predefined value of the cylinder high register destination and a third predefined value of the cylinder low register destination.

9.   (Original)   The method of claim 4, wherein two IDE drives may be connected per intelligent drive electronics channel and wherein a one of the IDE drives comprises a master drive and a one of the IDE drives comprises a slave drive.

10.   (Original)   The method of claim 9, wherein the drive selection value represents at least one of the master drive and the slave drive.

11.   (Original)   The method of claim 4 further comprising, prior to reading a status register destination, resetting the computer.

12.   (Original)   The method of claim 11, wherein resetting the computer comprises executing at least one of the following:

a power on reset of the computer;

a hardware reset;

an execute drive diagnostics command;

a software reset; and

a drive reset.

13.   (Original)   The method of claim 1, wherein the IDE drive comprises at least one of the following:

a hard disk drive;

a floppy drive;

a CD ROM disk drive; and

a tape drive.

14.   (Currently Amended) A computer program product comprising a computer storage medium having control logic stored therein for causing a computer to detect whether an IDE drive is connected to an intelligent drive electronics channel within the computer, said control logic comprising computer readable program code means for causing the computer to:

establish a drive selection value for each IDE drive wherein each IDE drive comprises at least one of a master IDE device and a slave IDE device;

select the IDE drive for detection by writing data to a drive head register destination for the IDE drive wherein the data includes the drive selection value established for the IDE drive;

in response to writing the data to the drive head register destination, read the drive head register destination;

detect whether the data read from the drive head register destination matches the data written to the drive head register destination;

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in response to the data read from the drive head register destination not matching the data written to the drive head register destination, return a first indication that the IDE drive is not connected to the intelligent drive electronics channel;

in response to the data read from the drive head register destination matching the data written to the drive head register destination, read the status register destination for the IDE drive;

detect whether data read from the status register destination has a first predefined value; ~~and~~

upon the data read from the status register destination not having the first predefined value, return a second indication that an IDE drive is connected to the intelligent drive electronics channel<u>;</u>

<u>upon the data read from the status register destination having the first predefined value, read a cylinder low register destination and a cylinder high register destination for the IDE drive;</u>

<u>detect whether data read from the cylinder low register destination and the cylinder high register destination matches a predefined signature; and</u>

<u>in response to the data read from cylinder low register destination and the cylinder high register destination matching the predefined signature, return the second indication that the IDE drive is connected to the intelligent drive electronics channel.</u>

15.   (Cancelled).

16.   (Cancelled).

17.   (Currently Amended) The computer program product of claim ~~16~~<u>14</u>, wherein the IDE drive connected to the intelligent drive electronics channel implements a packet command feature set.

18.   (Currently Amended) The method of claim ~~16~~<u>14</u>, wherein the predefined signature comprises a second predefined value of the cylinder high register destination and a third predefined value of the cylinder low register destination.

19.   (Currently Amended) A computer system for detecting whether an IDE drive is connected to an intelligent drive electronics channel within the computer system, the computer system comprising:

a processor coupled to a memory;

at least one bus coupled to the processor and capable of hosting at least one IDE drive via an intelligent drive electronics channel; and

a basic input/output system program capable of being executed on the processor and, when executed on the processor, operative to:

establish a drive selection value for each IDE drive wherein each IDE drive comprises at least one of a master IDE device and a slave IDE device;

select the IDE drive for detection by writing data to a drive head register destination for the IDE drive wherein the data includes the drive selection value established for the IDE drive;

in response to writing the data to the drive head register destination, read the drive head register destination;

detect whether the data read from the drive head register destination matches the data written to the drive head register destination;

in response to the data read from the drive head register destination not matching the data written to the drive head register destination, return a first indication that the IDE drive is not connected to the intelligent drive electronics channel;

in response to the data read from the drive head register destination matching the data written to the drive head register destination, read the status register destination;

detect whether data read from the status register destination has a first predefined value; ~~and~~

upon the data read from the status register destination not having the first predefined value, return a second indication that an IDE drive is connected to the intelligent drive electronics channel

upon the data read from the status register destination having the first predefined value, read a cylinder low register destination and a cylinder high register destination for the IDE drive;

detect whether data read from the cylinder low register destination and the cylinder high register destination matches a predefined signature; and

in response to the data read from cylinder low register destination and the cylinder high register destination matching the predefined signature, return the second indication that the IDE drive is connected to the intelligent drive electronics channel.

20. (Cancelled).

21. (Cancelled).

22. (Withdrawn) A method for detecting whether an ATAPI device is connected to an intelligent drive electronics channel within a computer, comprising:

reading a cylinder high register destination and a cylinder low register destination for the ATAPI device; and

based on a first value read from the cylinder high register destination and a second value read from the cylinder low register destination, determining whether the ATAPI device is connected.

23. (Withdrawn) The method of claim 22, wherein determining whether the ATAPI device is connected comprises:

detecting whether data read from the cylinder high register destination has a first predefined value and whether data read from the cylinder low register destination has a second predefined value; and

upon the data read from the cylinder high register destination having the first predefined value and the data read from the cylinder low register destination having the second predefined value, returning that the ATAPI device is connected to the intelligent drive electronics channel.

24. (Withdrawn) The method of claim 23, prior to reading at least one of the cylinder high register destination and the cylinder low register destination, further comprising:

reading a status register destination for the ATAPI device; and

detecting that the data read from the status register destination has a third predefined value.

25.   (Withdrawn) The method of claim 23, prior to reading the status register destination further comprising:

establishing a device selection value for one or more ATAPI devices wherein each ATAPI device comprises at least one of a master IDE device and a slave IDE device;

selecting the ATAPI device for detection by writing data to a device head register destination for the ATAPI device wherein the data includes the device selection value established for the ATAPI device;

reading the device head register destination after writing the data;

detecting whether the data read from the device head register destination matches the data written to the device head register destination; and

in response to the data read from the device head register destination matching the data written to the device head register destination, reading the status register destination.

26.   (Withdrawn) The method of claim 22, wherein the ATAPI device comprises at least one of the following:

a hard disk drive;

a floppy drive;

a CD ROM disk drive; and

a tape drive.

27.   (Withdrawn) A computer program product comprising a computer readable medium having control logic stored therein for causing a computer to detect whether an ATAPI drive is connected to an intelligent drive electronics channel within the computer, said control logic comprising computer readable program code means for causing the computer to:

read a cylinder high register destination and a cylinder low register destination for the ATAPI drive;

detect whether data read from the cylinder high register destination has a first predefined value and whether data read from the cylinder low register destination has a second predefined value; and

upon the data read from the cylinder high register destination having the first predefined value and the data read from the cylinder low register destination having the second predefined value, return an indication that the ATAPI drive is connected to the intelligent drive electronics channel.

28.   (Withdrawn) The computer program product of claim 27, prior to causing the computer to read at least one of the cylinder high register destination and the cylinder low register destination, further comprising computer readable program code means for causing the computer to:

read a status register destination for the ATAPI drive; and

detect that the data read from the status register destination has a third predefined value.

29.   (Withdrawn) A computer system operative to detect whether an ATAPI drive is connected to an intelligent drive electronics channel within the computer, said computer system comprising:

a processor coupled to a memory;

at least one bus coupled to the processor and capable of hosting at least one ATAPI drive via an intelligent drive electronics channel; and

a basic input/output system program capable of being executed on the processor and, when executed on the processor, operative to:

read a cylinder high register destination and a cylinder low register destination for the ATAPI drive;

detect whether data read from the cylinder high register destination has a first predefined value and whether data read from the cylinder low register destination has a second predefined value; and

upon the data read from the cylinder high register destination having the first predefined value and the data read from the cylinder low register destination having the second predefined value, return an indication that the ATAPI drive is connected to the intelligent drive electronics channel.

30.   (Withdrawn)   The computer system of claim 29, wherein prior to reading at least one of the cylinder high register destination and the cylinder low register destination, the basic input/output system program is further operative to:

read a status register destination for the ATAPI drive; and

detect that the data read from the status register destination has a third predefined value.